CLAIMS

What is claimed is:

1. A ring oscillator for generating a signal, comprising:

a semiconductor device package;

a semiconductor device used as an evaluation test chip physically attached to the semiconductor device package comprising;

an input pad circuit having an input signal and an output signal;

a buffering circuit having an input signal and an output signal, wherein the input signal of the buffering circuit is connected to the output signal of the input pad circuit; and

an output pad circuit having an input signal and an output signal, wherein the input signal of the output pad circuit is connected to the output signal of the buffering circuit;

a delay circuit having an input terminal operably coupled to the output signal of the output pad circuit and an output terminal operably coupled to the input signal of the input pad circuit, wherein the delay circuit alters the signal arrival time at the input signal of the input pad thereby modifying the frequency of the ring oscillator; and wherein the combination of all circuit elements in the ring oscillator creates an odd number of logic inversions.

2. The ring oscillator of claim 1, wherein the delay circuit comprises a circuit trace connection on the semiconductor device package of a predetermined length between the input terminal and the output terminal.

3. The ring oscillator of claim 1, wherein the delay circuit comprises at least one passive electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal.

4. The ring oscillator of claim 1, wherein the delay circuit comprises:

at least one active electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal; and

an enabling circuit operably coupled as part of the ring oscillator controlling activation of the ring oscillator.

5. The ring oscillator of claim 1, wherein the delay circuit comprises:

at least one passive electrical element and at least one active electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal; and

an enabling circuit operably coupled as part of the ring oscillator controlling activation of the ring oscillator.

6. A ring oscillator for generating a clock signal, comprising:

a circuit board;

a semiconductor device package physically attached to the circuit board;

a semiconductor device used as an evaluation test chip physically attached to the semiconductor device package comprising;

an input pad circuit having an input signal and an output signal;

a buffering circuit having an input signal and an output signal, wherein the input signal of the buffering circuit is connected to the output signal of the input pad circuit; and

an output pad circuit having an input signal and an output signal, wherein the input signal of the output pad circuit is connected to the output signal of the buffering circuit;

a delay circuit, having an input terminal operably coupled to the output signal of the output pad circuit and an output terminal operably coupled to the input signal of the input pad circuit, wherein the delay circuit alters the signal arrival time at the input signal of the input pad thereby modifying the frequency of the ring oscillator; and wherein the combination of all circuit elements in the ring oscillator creates an odd number of logic inversions.

7. The ring oscillator of claim 6, wherein the delay circuit comprises a circuit trace connection on the circuit board of a predetermined length between the input terminal and the output terminal.

8. The ring oscillator of claim 6, wherein the delay circuit comprises at least one passive electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal.

9. The ring oscillator of claim 6, wherein the delay circuit comprises:

at least one active electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal; and

an enabling circuit operably coupled as part of the ring oscillator controlling activation of the ring oscillator.

10. The ring oscillator of claim 6, wherein the delay circuit comprises:

at least one passive electrical element and at least one active electrical element operably connected in a manner creating a predetermined time delay between the input terminal and the output terminal; and

an enabling circuit operably coupled as part of the ring oscillator controlling activation of the ring oscillator.

11. A method for modifying a frequency of an oscillating signal comprising:

generating an oscillating signal of a predetermined frequency on a semiconductor device used as an evaluation test chip, wherein a predetermined number of circuit elements on the semiconductor device are connected in a ring oscillator configuration; and

modifying the predetermined frequency of the oscillating signal by operably coupling a delay element in the ring oscillator configuration, wherein the operable coupling occurs on a semiconductor device package containing the semiconductor device.

12. The method of claim 11, wherein the step of modifying the predetermined frequency comprises, modifying a time delay of the delay element by combining at least one circuit element selected from the group consisting of, circuit traces, passive electrical elements, and active electrical elements.

13. The method of claim 11 further comprising, enabling operation of the oscillating signal in response to a control signal.

14. The method of claim 13, wherein the step of modifying the predetermined frequency comprises, modifying a time delay of the delay element by combining at least one circuit element selected from the group consisting of, circuit traces, passive electrical elements, and active electrical elements.

15. A method for modifying a frequency of an oscillating signal comprising:

generating an oscillating signal of a predetermined frequency on a semiconductor device used as an evaluation test chip, wherein a predetermined number of circuit elements on the semiconductor device are connected in a ring oscillator configuration; and

modifying the predetermined frequency of the oscillating signal by operably coupling a delay element in the ring oscillator configuration, wherein the operable coupling occurs on a circuit board containing the semiconductor device.

16. The method of claim 15, wherein the step of modifying the predetermined frequency comprises, modifying a time delay of the delay element by combining at least one circuit element selected from the group consisting of, circuit traces, passive electrical elements, and active electrical elements.

17. The method of claim 15 further comprising, enabling operation of the oscillating signal in response to a control signal.

18. The method of claim 17, wherein the step of modifying the predetermined frequency comprises, modifying a time delay of the delay element by combining at least one circuit element selected from the group consisting of, circuit traces, passive electrical elements, and active electrical elements.

19. A ring oscillator for generating a signal, comprising:

a means for generating an oscillating signal of a predetermined frequency on a semiconductor device used as an evaluation test chip, wherein a predetermined number of circuit elements on the semiconductor device are connected in a ring oscillator configuration; and

a means for modifying the predetermined frequency of the oscillating signal by operably coupling a delay element in the ring oscillator configuration, wherein the operable coupling occurs on a semiconductor device package containing the semiconductor device.

20. A ring oscillator for generating a signal, comprising:

a means for generating an oscillating signal of a predetermined frequency on a semiconductor device used as an evaluation test chip, wherein a predetermined number of circuit elements on the semiconductor device are connected in a ring oscillator configuration; and

a means for modifying the predetermined frequency of the oscillating signal by operably coupling a delay element in the ring oscillator configuration, wherein the operable coupling occurs on a circuit board containing the semiconductor device.